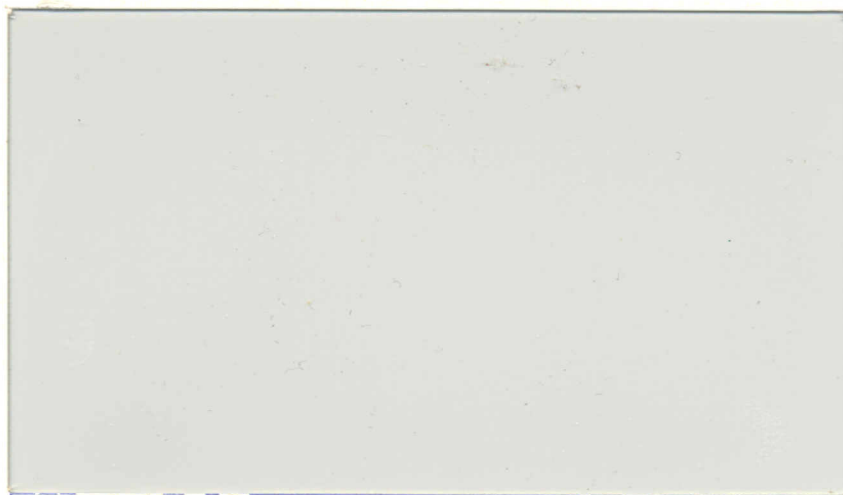




Product - QBX-MSP
Product Number - 1184 (MSP/2), 1185 (MSP/4)
Manual Number - 1184-01

Change History	
Rev	Description
1.0	Initial Document

QBX-MSP
MULTI SERIAL PORT
USER MANUAL

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Q & D Electronics (Pty) Ltd,
P.O. Box 2100,
Waterloo, Ontario, Canada
N2L 2G1, Canada
Telephone: 514-594-1141

QBX-MSP

Product:- QBX-MSP

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Manual Number:- 1004-01

Chapter	Rev	Note
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P.O. Box 61903,
Marshalltown 2107,
Johannesburg, South Africa.
Telex: 8-3046 Phone: 834-1204

Rev:1.0

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CHAPTER 1 GENERAL

Introduction

The QBX-MSP board is one of a growing range of iSBX bus compatible boards manufactured by Quantum Electronics. These boards are designed to increase the number of functions on a Multibus system without having to resort to the addition of a full Multibus card to achieve that function. This document provides all the information required to use the QBX-MSP.

Description

Advances in semiconductor technology have allowed the realisation of many sophisticated communications controllers. One such device is the Western Digital WD2123. This device consists of 2 micro-processor compatible UARTs (universal asynchronous receiver transmitter) and 2 independent baud rate generators in a single 40 pin DIL package. The QBX-MSP/4 has 2 such devices on the card, whilst the QBX-MSP/2 is a depopulated version with only 1 device. Coupled with RS232 drivers and receivers the QBX-MSP/4 provides 4 RS232 channels on a double sized iSBX compatible board. There is also a facility for the generation of interrupts, and if there is an unused channel the spare baud rate generator may be used for periodic interrupts.

Equipment Supplied

The QBX-MSP is shipped in a padded package. Included in this package are 2 plastic spacers and 4 plastic screws to mount the board on the host SBC type board.

The QBX-MSP/2 is a depopulated version of the QBX-MSP/4. However it may NOT be upgraded to the MSP/4 by merely adding a WD2123 and receiver/transmitter as the decoding programmed in the PAL (programmed array logic) differs between the two.

The output from the QBX-MSP is via an edge connector. Quantum Electronics also produce a board with 2 or 4 25 way D-type connectors that connects to the QBX-MSP via a ribbon cable. This board is designated QBN-MSP-CON.

Specifications

Access Time:

Both read and write 600-700ns

Addressing Range:

The QBX-MSP is compatible with any board that supports the Intel iSBX bus. The addressing range of the QBX-MSP is derived from this host board.

Interface:

Serial Bus 2 Drivers per channel RTS and TxD

2 Receivers per channel CTS and RxD

System Bus Compatible with the SBX bus specifications. See Intel publication 142686-001.

Interface connectors:

13/26 way, 0.1 in spacing, compatible with Robinson Nugent IDE-26 or similar

Power Requirements:

+5 Volt +/- 5% @537mA (MSP/2 @411mA)

+12 Volt +/- 10% @53mA (MSP/2 @26mA)

-12 Volt +/- 10% @46mA (MSP/2 @23mA)

Environment:

Operating temperature 0-55 degrees centigrade, humidity to 90% non condensing

Size:

Width 724 mm (2.85 in)

Length 1900.5 mm (7.5 in)

Height 17.5 mm (0.69 in) Components plus QBX connector.

Weight

CHAPTER 2 PRINCIPLE OF OPERATION

Introduction

This chapter describes how the QBX-MSP operates. Detailed description of the operation of the WD2123 UART is presented in appendix A.

QBX Bus Interface

Detailed description of the iSBX bus is contained in the Intel publication 142686-001. Users are referred to this document for a thorough description of this bus. The QBX-MSP uses the following signals: MD0-MD7, MA0-MA2, CS0/, CS1/, IOWRT/, IORD/, MINTR0, MINTR1, MPST/, MCLK, MWAIT/, MRESET, and of course, +12v, -12v, +5v, and ground.

Access Time

Worst Case Conditions for the WD2123 requires the address and chip selects to be valid a minimum of 50nS prior to Read or Write. The iSBX bus specification only allows for 50 nS; due to propagation delays we would therefore violate this requirement if we were to connect the QBX commands to the WD2123 command lines. Further the minimum command pulse widths are 350nS, longer than the value for the iSBX bus. In addition the WD2123 requires a data hold time of 100nS after the termination of the write signal. This too, is not compatible with the SBX bus. the data hold time after a read signal is 200nS again exceeding the bus specification.

In order to circumvent these potential problems extra circuitry is introduced to the design to generate pseudo command signals. Whenever either UART is accessed, U9/18 (ONBD/) goes low. Whilst a UART is not accessed the 8 bit serial to parallel shift register (U5) is held reset with its outputs at zeroes. When ONBD/ goes active this shift register is enabled, and every 100nS a "1" is shifted along the outputs.

Read Cycle

Whenever a Read to the UARTs is performed, this signal is delayed by gating it with the QB output of U5. This delay is 100-200nS. As ONBD/ goes active it enables the buffer U13 and /MWAIT and stays enabled for 600-700nS until QG (U5/12) goes high. This terminates the read cycle, and also disables the 74LS245 so that the data read hold time does not interfere with SBX bus.

Write Cycle

When a write to the UART occurs the actual write signal is delayed as above, enabling the buffer U13 and generating a wait condition. When QF of the shift register U5 goes high, it drives the pseudo write(/WR') inactive, terminating the write to the device. As far as the SBX bus is concerned however, the write is still in progress until the /MWAIT goes inactive, which occurs

100ns later. This allows the delays to meet the requirements of both the SBX and the WD2123 buses.

Address Decoding

The decoding for the different chip selects is achieved using a PAL (Programmed Array Logic). The programming differs from the MSP/4 to the MSP/2.

Table 2.1 provides the relevant addresses for the different registers in the 2 WD2123s.

I/O Address	RD/	WR/	Function
ABCD0000	0	1	Channel A Receiver Holding Register
ABCD0000	1	0	Channel A Transmit Holding Register
ABCD0001	0	1	Channel A Status Register
ABCD0001	1	0	Channel A Mode and Command Register
ABCD0010	0	1	Channel B Receiver Holding Register
ABCD0010	1	0	Channel B Transmit Holding Register
ABCD0011	0	1	Channel B Status Register
ABCD0011	1	0	Channel B Mode and Command Register
ABCD0100	1	0	Channel A Rate Register
ABCD0101	1	0	Channel B Rate Register
Continuation only for MSP/4			
ABCD1000	0	1	Channel C Receiver Holding Register
ABCD1000	1	0	Channel C Transmit Holding Register
ABCD1001	0	1	Channel C Status Register
ABCD1001	1	0	Channel C Mode and Command Register
ABCD1010	0	1	Channel D Receiver Holding Register
ABCD1010	1	0	Channel D Transmit Holding Register
ABCD1011	0	1	Channel D Status Register
ABCD1011	1	0	Channel D Mode and Command Register
ABCD1100	1	0	Channel C Rate Register
ABCD1101	1	0	Channel D Rate Register

Table 2.1
I/O addresses for function registers on QBX-MSP

Note:

ABCD are bit values that are determined by the host board.
For RD/ and WR/ 0 indicates an active signal.

Interrupts

Each communication channel has 4 outputs capable of generating an interrupt. Table 2.2 lists the pin function with the associated jumper label. These jumpers may be user configured to create an interrupt to the system on MINT0, through the PAL which is programmed to act as a 6 input OR gate. Remember to ground all unused

inputs to this OR gate. The inputs to the OR gate are denoted by the letters S to X inclusive. The grounding pads are denoted Y,Z,AA,AB,AC. The interrupt is enabled to the QBX connector by joining the link AF to AE.

If Channel B or D is not being used the baud rate generator output may be used to generate periodic interrupts on MINT1. To do this jumper AJ (channel D) or AG (channel B) to AH.

Jumper pad label	Function
J	TXRDY Channel D
K	RXRDY Channel D
L	TXE Channel D
M	BRKDET Channel D
N	TXRDY Channel C
P	RXRDY Channel C
Q	TXE Channel C
R	BRKDET Channel C
A	TXRDY Channel B
B	RXRDY Channel B
C	TXE Channel B
D	BRKDET Channel B
E	TXRDY Channel A
F	RXRDY Channel A
G	TXE Channel A
H	BRKDET Channel A
AG	XCI/BCO Channel B
AJ	XCI/BCO Channel D
AF	Interrupt output
AD	Inverted AF above
AH	Connected to MINT1
AE	Connected to MINT0

Table 2.2
Jumper Pad Identification

RS232 Interface

Each channel is interfaced to the RS232 levels by appropriate buffers. The outgoing signals TxD and RTS are buffered to +/- 12v by a 1488 driver, and the incoming signals RxD and CTS are buffered by a 1489. Facilities exist for the placing of noise reducing capacitors (C9-C16) and slew rate capacitors (C1-C8) on the QBX-MSP. However, the product is shipped without these capacitors installed. Unused inputs of the receiving device, (terminal, printer etc.) such as DTR or even CTS if it is not being used should be connected to the 150 ohm pull up resistor to enable these functions. The RS232 signals are brought

out to a 26 way edge connector. The pin allocation is shown in table 2.3.

Connector Number	Function
1	Gnd
2	+12v pullup
3	CTS Channel C
4	RxD Channel C
5	RTS Channel C
6	TxD Channel C
7	Gnd
8	+12v pullup
9	CTS Channel D
10	RxD Channel D
11	RTS Channel D
12	TxD Channel D
13	Gnd
14	+12v pullup
15	CTS Channel A
16	RxD Channel A
17	RTS Channel A
18	TxD Channel A
19	Gnd
20	+12v pullup
21	CTS Channel B
22	RxD Channel B
23	RTS Channel B
24	TxD Channel B
25	not used
26	not used

Table 2.3
RS232 connector pinout

In order to facilitate connection of 25 way D-type connectors to the QBX-MSP Quantum Electronics also manufactures the QBN-MSP-CON. This board has 4 (or 2) RS232 type connectors with a "configurator" for each connector. It is connected to the QBX-MSP via a ribbon cable, for quick and reliable connection.

Oscillator

A 1.8432MHz crystal is connected across a CMOS Schmitt trigger input NAND gate to cause it to oscillate at its resonant frequency. These oscillations are buffered and drive both WD2123s. Whilst the frequency is not calibrated prior to shipping it should be within +/- 0.1%. If this is too wide, a variation

the frequency may be trimmed by adding a trimmer in the location marked VC1. Beware however, that the overall height of the board will not exceed 0.4 inches as this may foul the board above the host board.

CHAPTER 3 PROGRAMMING INFORMATION

Most of the programming information is contained in appendix A. The user should take note of the following facts.

1. In order to use the circuitry as configured on the board, for each channel bit CR1 (CS) in the command register must be set to a "1". The SELCLK pins are all held high so that the clocks are driven from the internal baud rate generator. XCI/BCO becomes an output driven by the baud rate generator.
2. When initialising the WD2123 be wary of the software reset function. If this occurs as a first instruction after a hardware reset, unpredictable results may occur. This is more obvious when working with in circuit emulation, and software has been written for the case where a reset is setting the programme counter to 0. It has been found empirically that writing the software reset twice in succession allows a reset to occur both through the hardware signal and the software instruction.

When using a host SBC computer reading and writing is simply executing an IN or OUT instruction (respectively) to the appropriate address. The rest of the operation is transparent to the host computer except that several wait states are generated.

Quantum Electronics also manufacture a board entitled "QBC-QBX" which is an SBC compatible board with connectors for up to 4 QBX boards. It also allows these boards to be configured as I/O mapped or memory mapped.

CHAPTER 4 PREPARATION FOR USE

Introduction

This chapter provides information on the installation of the QBX-MSP on a host SBC board.

Unpacking

The QBX-MSP is shipped in a padded packet together with 2 plastic spacers and 4 plastic screws.

On receipt of the package inspect immediately for signs of damage, water or any other signs of mishandling. If there are any of these signs contact your carrier or his agent, or the local Quantum Electronics representative. If you do open the package, please retain the packaging.

Mounting

The QBX-MSP will mount on any SBC computer that allows a double sized ISBX board. Affix the two spacers with two of the screws to the host board. Quantum Electronics suggests you mount one in the location that corresponds to the hole just to the right of the edge connector. The second should be mounted in the location corresponding to the hole on the QBX-MSP to the right and slightly higher than the crystal.

The QBX-MSP should now be mounted on the mating connector and affixed to the host board with the remaining two screws.

When a QBX card is mounted on a host card, the resulting structure occupies an additional card slot above the SBC card. Bear this in mind when you allocate slots in a cardframe.

X

CHAPTER 5 SERVICE

Introduction

This chapter provides a parts list and a schematic diagram of the QBX-MSP.

Parts List

Semiconductors:

U1,3*	RS232 line driver	MC1488
U2,4*	RS232 line receiver	MC1489
U5	serial to pll s.r.	74164
U6,12	quad NAND gate	74LS00
U7,8*	UART	WD2123
U9	programmed part	PAL 10L8
U10	quad CMOS NAND gate with Schmitt inputs	4093
U11	quad NOR gate	74LS02
U13	octal buffer	74LS245

Capacitors:

C17-20,23	ceramic	0.01uF
C21	ceramic	10pF
C22	ceramic	22pF

Resistors:

R1-4	1/4 Watt 5%	150 ohms
R5	1/4 Watt 5%	22 Kohms 10M

Crystal:

X1	pll resonant crystal	1.8432 MHz
----	----------------------	------------

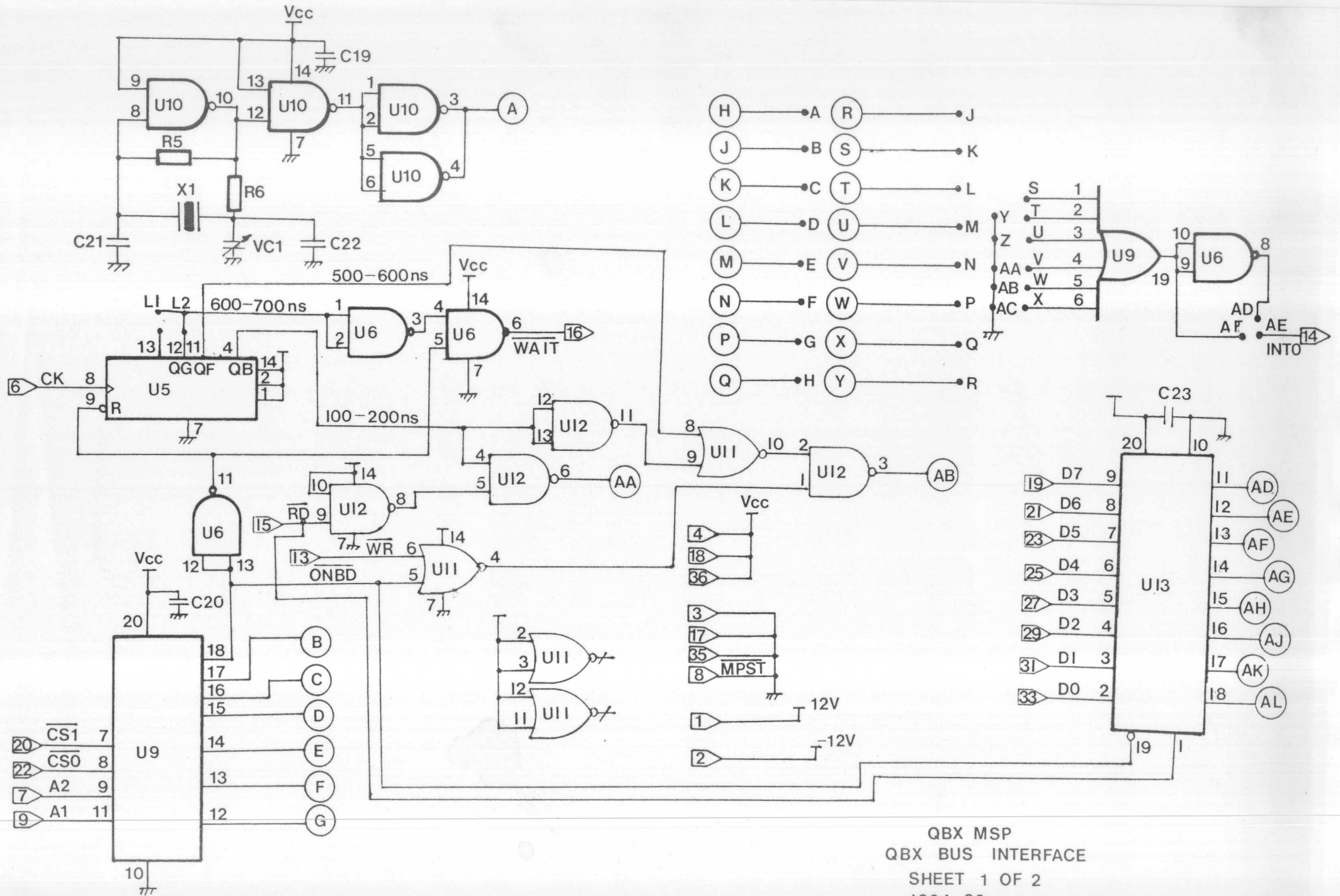
Connector:

36 way SBX	Viking LMP01KH18A01
------------	---------------------

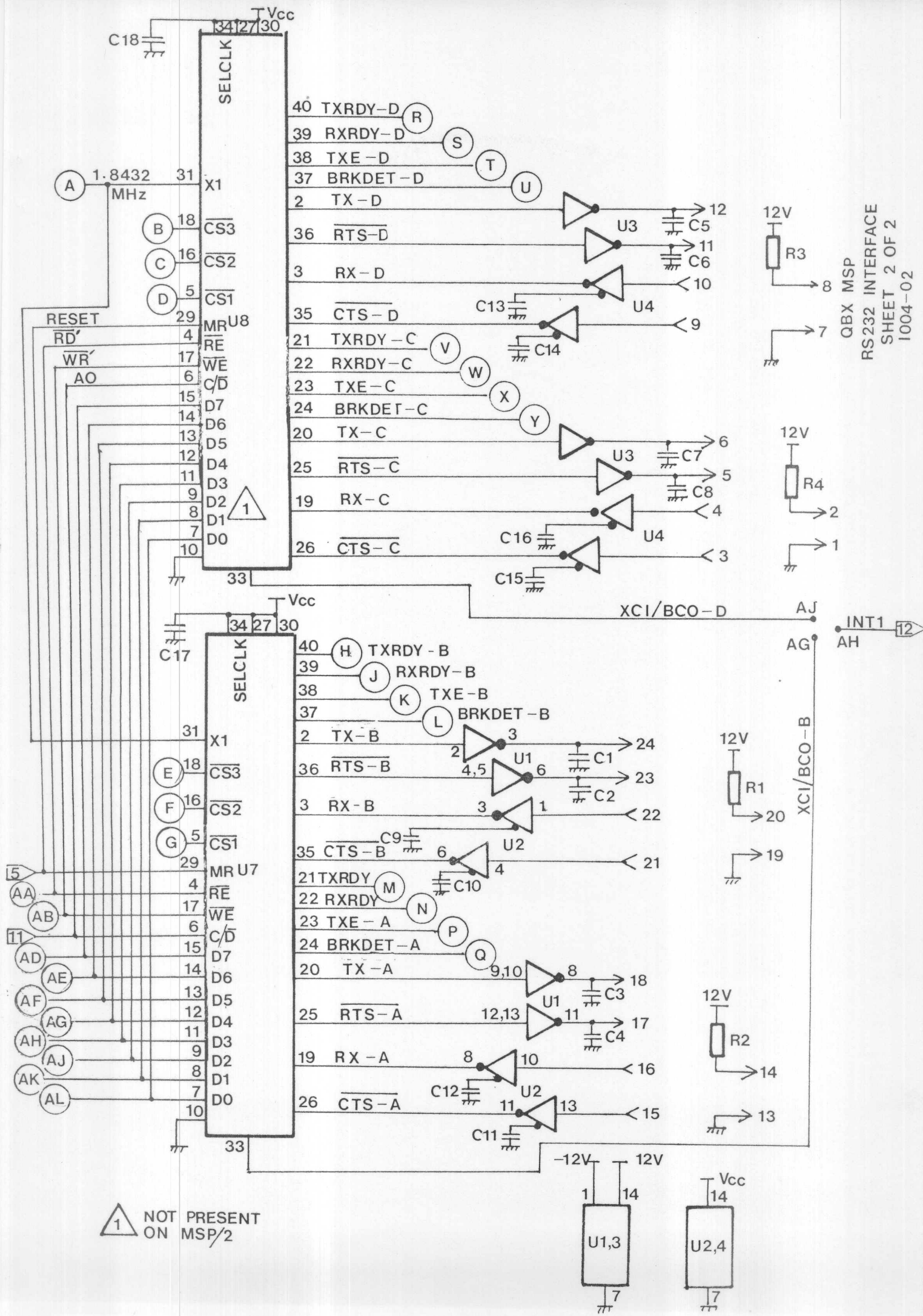
Unused parts:

VC1
R6
C1-16

* U3,4,8 not present on QBX-MSP/2



QBX MSP
QBX BUS INTERFACE
SHEET 1 OF 2
1004-02
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RS232 INTERFACE
SHEET 2 OF 2
1004-02

APPENDIX A
WD2123 DATA SHEET

The following pages are extracted from the WD2123 data sheet.

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PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
10	GROUND	VSS	Ground
30	POWER SUPPLY	VCC	+5VDC power supply input.
7	DATA BUS	D0	This is the 8 bit Bidirectional Data Bus. It is the means of communication between the WD2123 and the CPU. Data, control, mode and status registers are accessed via this bus.
8		D1	
9		D2	
11		D3	
12		D4	
13		D5	
14		D6	
15		D7	
5	CHIP SELECT ONE	$\overline{CS1}$	V_{IL} on this input selects Channel A and enables computer communications with Channel A Data, control and status registers.
16	CHIP SELECT TWO	$\overline{CS2}$	V_{IL} on this input selects Channel B and enables computer communications with Channel B Data, control and status registers.
18	CHIP SELECT THREE	$\overline{CS3}$	V_{IL} on this input select the Baud Rate registers for programming.
6	CONTROL or DATA SELECT	$C/\overline{D}$	This input is used in conjunction with the appropriate Chip Select and an active read or write operation to determine register access via the Data Bus.
4	READ ENABLE	$\overline{RE}$	V_{IL} on this input allows the CPU to read data, or status information from the selected register.
17	WRITE ENABLE	$\overline{WE}$	V_{IL} on this input allows the CPU to write data or control information into the selected register.
29	MASTER RESET	MR	V_{IH} on this input resets both channels to the idle state and resets the status, command, mode and Data registers.
31	CRYSTAL OSCILLATOR INPUT	XTAL1	This is the input side of the on-chip oscillator. It can also be driven by an external clock source.
32	CRYSTAL OSCILLATOR OUTPUT	XTAL2	This is the output side of the on-chip oscillator.
27	SELECT CLOCK (Channel A)	SELCLK-A	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel A.
34	SELECT CLOCK (Channel B)	SELCLK-B	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel B.
28	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT- (Channel A)	XC/BCO-A	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel A)
33	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel B)	XC/BCO-B	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel B)
26	CLEAR-TO-SEND (Channel A)	$\overline{CTS-A}$	V_{IL} on this input enables Channel A to transmit serial data if the Transmitter is enabled.
35	CLEAR-TO-SEND (Channel B)	$\overline{CTS-B}$	V_{IL} on this input enables Channel B to transmit serial data if the Transmitter is enabled.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
20	TRANSMIT DATA (Channel A)	TXD-A	This is the Serial Data Output from Channel A.
2	TRANSMIT DATA (Channel B)	TXD-B	This is the Serial Data Output from Channel B.
19	RECEIVE DATA (Channel A)	RXD-A	This is the Serial Data Input for Channel A.
3	RECEIVE DATA (Channel B)	RXD-B	This is the Serial Data Input for Channel B.
21	TRANSMITTER READY (Channel A)	TXRDY-A	This output, when high (V_{OH}), alerts the CPU that Channel A is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system.
40	TRANSMITTER READY (Channel B)	TXRDY-B	This output, when high (V_{OH}), alerts the CPU that Channel B is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system.
22	RECEIVER READY (Channel A)	RXRDY-A	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
39	RECEIVER READY (Channel B)	RXRDY-B	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
23	TRANSMITTER EMPTY (Channel A)	TXE-A	This output, when high (V_{OH}), indicates that Channel A Transmitter has no new characters to send and is waiting in an idle state.
38	TRANSMITTER EMPTY (Channel B)	TXE-B	This output, when high (V_{OH}), indicates that Channel B Transmitter has no new characters to send and is waiting in an idle state.
24	BREAK DETECT (Channel A)	BRKDET-A	This output, when high (V_{OH}), indicates that the Receiver for Channel A has detected a break condition.
37	BREAK DETECT (Channel B)	BRKDET-B	This output, when high (V_{OH}), indicates that the Receiver for Channel B has detected a break condition.
25	REQUEST-TO-SEND (Channel A)	$\overline{\text{RTS-A}}$	A general purpose output that is controlled by the command register bit CR5 for Channel A.
36	REQUEST-TO-SEND (Channel B)	$\overline{\text{RTS-B}}$	A general purpose output that is controlled by the command register bit CR5 for Channel B.
1		NC	No Internal Connection.

Table 1 WD2123 PIN DESCRIPTIONS

GENERAL DESCRIPTION

The WD2123 Block Diagram is shown in Figure 2. The WD2123 is a merger of two WD1983s and one WD1941 from WDC's line of communications devices on one piece of silicon. The 1983 is an asynchronous only version of the 8251A and the 1941 is a baud rate generator. In this manner, 8251A compatibility is maintained with the WD2123 with the added features of 2 channels and 2 baud rate generators on a single chip.

As depicted from the block diagram, the channels are referred to as CHANNELS A and B. CHANNEL A, which is an asynchronous 8251A, is addressed or controlled by the input signal $\overline{CS1}$. CHANNEL B is similarly controlled by $\overline{CS2}$. Finally, the BAUD RATE GENERATORS are controlled by $\overline{CS3}$.

Each channel of the WD2123 can be programmed to receive and transmit asynchronous serial data. The WD2123 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the status of either channel at any time. Status information on a per channel basis reported includes the type and the condition of the transfer operations being performed by the WD2123 as well as any transmission error conditions (parity, overrun, or framing). Programming the WD2123 is identical to the 8251A in the asynchronous mode, remembering that $\overline{CS1}$, when low, selects CHANNEL A and when $\overline{CS2}$ is low, selects CHANNEL B.

The WD2123 BAUD RATE GENERATORS may be selected either internally or externally. The clock select logic includes a clock select control bit CR1 (CS) in each COMMAND INSTRUCTION REGISTER. This control bit allows selection of the internal baud clock or an externally applied clock and works in conjunction with the select clock pin, "SELCLK" and the external clock input/baud clock output pin, "XCI/BCO". When CS is logic 1, the external clock select mode is selected. This means that the transmit and receive clocks (TXC and RXC) are internally tied together and the select clock pin, SELCLK, will determine whether those clocks are driven from the internal baud rate generator (SELCLK is high) or from the external clock input pin, "XCI/BCO", (SELCLK is low).

If the internal BRG clock is selected, (SELCLK is high) then the external clock input pin becomes a BRG clock output. Hence, the mnemonic, "XCI/BCO".

When CR1 (CS) is logic 0, then internal clock select mode is selected. The transmit clock (TXC) is driven by the internal BRG clock and the receive clock is driven by the select clock pin, (SELCLK). The XCI/BCO pin becomes the baud clock output (the same signal that is being applied to TXC).

The WD2123 also provides a local loop-back test mode of operation for each channel. This diagnostic mode is independently controlled via the LB(CR7) bit of the COMMAND REGISTER. When LB is logic 1, the channel is programmed

for Local Loop-Back. In this diagnostic mode, the TXD output is set to the marking (logic "1") state; the output of the TRANSMIT REGISTER is "looped-back" into the RECEIVER REGISTER input; $\overline{RTS}$ output is held high; the $\overline{CTS}$ and RXD inputs are ignored. An additional requirement is that the TEN(CR0) command bit and the REN(CR2) be logic 1. The status and output flags operate normally.

Each channel is also provided with break character generation and detection. (A break character is defined as all zero data bits, parity bit and stop bits after a valid start bit.) For break character generation, SBRK (CR3) command bit is set to a logic 1. This causes the TXD output to be forced low (spacing) for as long as SBRK is programmed high. The break detect output and status bit (SR6) is set to logic 1, indicating that the receiver has detected a break character. The framing error flag is also set to 1 for this condition.

ORGANIZATION

The WD2123 is an eight bit bus-oriented device. Communication between the controlling CPU and the two RECEIVER/TRANSMITTER CHANNELS or the two BAUD RATE GENERATORS occurs via the 8 bit data bus through a common set of bus transceivers.

A diagram of one of the two communication controllers is shown in Figure 3. There are two accessible data registers, which buffers transmit and receive data. They are the TRANSMIT HOLDING REGISTER and the RECEIVE HOLDING REGISTER. There is a parallel-to-serial shift register, the TRANSMIT REGISTER and a serial-to-parallel shift register, the RECEIVE REGISTER.

Operational Control and monitoring of the CHANNEL is performed by two CONTROL REGISTERS (the COMMAND INSTRUCTION REGISTER and the MODE INSTRUCTION REGISTER) and the STATUS REGISTER.

A read/write control circuit allows programming/monitoring or loading/reading of data in the CONTROL, STATUS and HOLDING REGISTERS by activating the appropriate control lines: Chip Select ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$), READ ENABLE ($\overline{RE}$), WRITE ENABLE ($\overline{WE}$) and CONTROL or DATA SELECT ($C/\overline{D}$).

Internal control of each channel is by means of two internal microcontrollers: one for transmit and one for receive. The control registers, various counters and external signals provide inputs to the microcontrollers, which generate the necessary control signals to send and receive serial data according to the programmed protocol.

A diagram of one of the two BAUD RATE GENERATORS is shown in Figure 4. The 4 low order DATA BUS bits, DO-D3, are used to program the desired rate by loading the RATE REGISTER. Control signals $\overline{CS3}$, $\overline{WE}$ and $C/\overline{D}$ are used to select and load the appropriate register.

The contents of the RATE REGISTER is decoded and addresses a FREQUENCY SELECT ROM for the proper frequency, which is generated by the DIVIDER circuitry and the control logic.

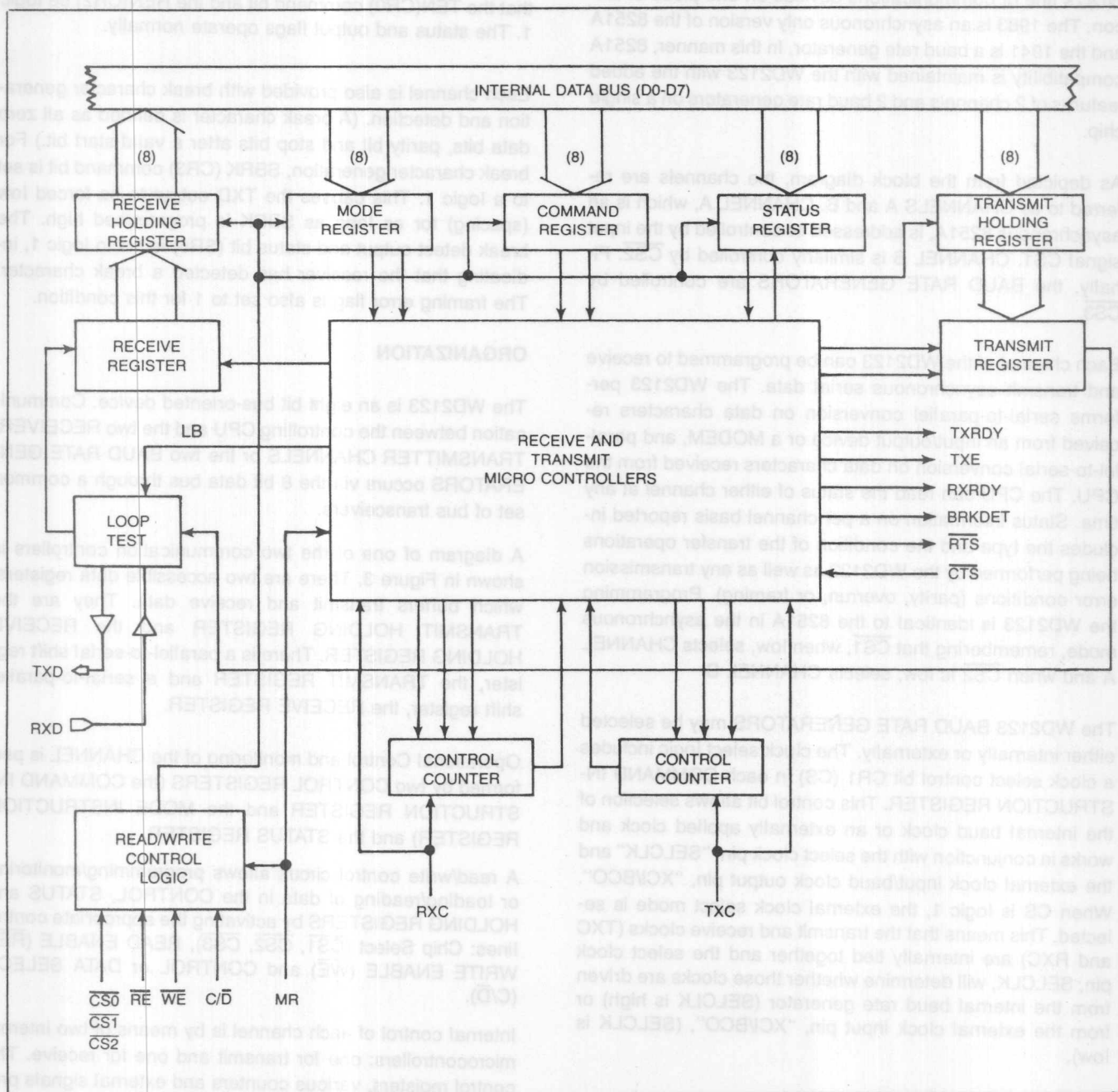


Figure 3. RECEIVE/TRANSMIT COMMUNICATIONS CONTROLLER DIAGRAM

The WD2123 contains two MODE REGISTERS—one for each channel. The format and definition of the MODE REGISTERS are shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
S2	S1	EP	PEN	L2	L1	B2	B1

B2	B1	BAUD RATE FACTOR
0	0	Undefined
0	1	1X
1	0	16X
1	1	64X
L2	L1	CHARACTER LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits
PEN	PARITY ENABLE	
0	Disable Parity	
1	Enable Parity	
EP	PARITY SELECT	
0	Odd Parity	
1	Even Parity	
S2	S1	NUMBER OF STOP BITS
0	0	Invalid
0	1	1 Bit
1	0	1½ Bits
1	1	2 Bits

Table 3 WD2123 MODE REGISTERS

The WD2123 contains two COMMAND REGISTERS—one per channel. The format and definition of the COMMAND REGISTERS are shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
LB	IR	RTS	ER	SBK	REN	CS	TEN

TEN	TRANSMIT ENABLE
1	Enable
0	Disable
CS	CLOCK SELECT
1	External Clock Select Mode
0	Internal Clock Select Mode
REN	RECEIVE ENABLE
1	Enable
0	Disable
SBK	SEND BREAK CHARACTER
1	Force TXD Low
0	Normal Operation
ER	ERROR RESET
1	Reset Error Flags
0	No Reset
RTS	REQUEST TO SEND
1	Force $\overline{\text{RTS}}$ pin = 0 (V_{OL})
0	Force $\overline{\text{RTS}}$ pin = 1 (V_{OH})
IR	INTERNAL RESET
1	Returns WD2123 to Mode Instruction Format
LB	LOOP BACK ENABLE
0	Normal Operation Mode
1	Local Loop-Back Mode

Table 4 WD2123 CONTROL REGISTERS

The WD2123 contains two STATUS REGISTERS—one per channel. The STATUS REGISTER is a read-only register. The format and definition of the STATUS REGISTERS are shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
CTS	BRK DET	FE	OE	PE	TXE	RX RDY	TX RDY

TXRDY		TRANSMITTER READY	
1		Denotes THR is empty and ready for a new character	
0		THR not empty. (Reset when THR is loaded by CPU)	
RXRDY		RECEIVER READY	
1		Denotes that the RHR contains a valid character	
0		RHR does not contain a valid character. (Reset when the CPU reads the RHR)	
TXE		TRANSMITTER EMPTY	
1		Denotes that the TR is empty	
0		Denotes that the TR is not empty	
PE		PARITY ERROR	
1		Denotes Parity Error	
0		No Parity Error. (Reset by ER bit of command register)	
OE		OVERRUN ERROR	
1		Denotes Overrun Error	
0		No Overrun Error. (Reset by ER bit of command register)	
FE		FRAMING ERROR	
1		Denotes Framing Error	
0		No Framing Error. (Reset by ER bit of command register)	
BRKDET		BREAK DETECT	
1		Indicates that the receiver has detected a line break condition. (FE will also be set)	
0		No Break Condition detected for at least one bit time	
CTS		CLEAR-TO-SEND	
1		Indicates that the $\overline{\text{CTS}}$ pin is active (V_{IL})	
0		Indicates that the $\overline{\text{CTS}}$ pin is not active (V_{IH})	

Table 5 WD2123 STATUS REGISTERS

The WD2123 contains two RATE REGISTERS that are used to select 16 BAUD rates when CR1 = 1 and SELCLK = 1. The Format of the RATE REGISTERS is shown below. Note that the Receiver and the Transmitter of any channel run off the same Baud clock except when CR1 = 0, then the Transmitter runs off the Baud Clock and the Receiver runs off an externally applied signal input on the SELCLK pin.

D7							D0
X	X	X	X	RA3 RB3	RA2 RB2	RA1 RB1	RA0 RB0

When C/D=0, RA3 to RA0 are loaded.
When C/D=1, RB3 to RB0 are loaded.

The C/D line is used in conjunction with CS3 and WE to program the desired BAUD rate. When C/D is low, Channel A is selected, and when C/D is high, Channel B is selected. The low order 4 bits of the DATA BUS are loaded into the selected rate register, and the high order 4 bits are ignored.

When the crystal frequency equals 1.8432 MHz, the following baud rates may be programmed.

R3	R2	R1	R0	BAUD RATE	FREQUENCY
0	0	0	0	50	.800 KHZ
0	0	0	1	75	1.200
0	0	1	0	110	1.760
0	0	1	1	134.5	2.150
0	1	0	0	150	2.400
0	1	0	1	200	3.200
0	1	1	0	300	4.800
0	1	1	1	600	9.600
1	0	0	0	1200	19.200
1	0	0	1	1800	28.800
1	0	1	0	2400	38.400
1	0	1	1	3600	57.600
1	1	0	0	4800	76.800
1	1	0	1	7200	115.200
1	1	1	0	9600	153.600
1	1	1	1	19,200	307.200

Table 6 WD2123 BAUD RATE REGISTERS

OPERATING DESCRIPTION

The WD2123 is primarily designed to operate in an 8 bit microprocessor environment, although other control logic schemes are easily implemented. The DATA BUS and the interface control signals ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{C/D}$, $\overline{RE}$, $\overline{WE}$) should be connected to the microprocessor's data bus and system control bus. A 1.8432 MHz crystal should be connected to the WD2123 as shown in figure 5. The appropriate TXC (RXC) clock frequencies should be programmed via system software. Different Baud clock configurations are possible, such as separate transmit and receive frequencies, and are outlined in the general description.

For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits. Interface control signals, $\overline{CTS}$ and $\overline{RTS}$, are controlled and sensed by the CPU through the COMMAND and STATUS REGISTERS and can be configured in several ways. The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The TXRDY, RXRDY, TXE and BRKDET FLAGS may be connected to the microprocessor system as interrupt inputs or the STATUS REGISTER can be periodically read in a polled environment to support data communication control operations.

The SBRK bit of the COMMAND REGISTER (CR3) is used to send a Break Character. (A Break Character is defined as a start bit, and all zero data, parity and stop bits.) When the CR3 bit is set to a "1", it causes the transmitter output, TXD, to be forced low after the last bit of the last character is transmitted.

The Receiver is equipped with logic to look for a break character. When a break is received, the BREAK DETECT (BRKDET) FLAG and STATUS bit are set to "1". When the receiver input line goes high (V_{IH}) for at least one clock period, the receiver resets the BRKDET FLAG and resumes its search for a start bit.

PROGRAMMING PROCEDURE

The programming sequence of the two channels will be different, depending on whether it is an initialization sequence (that is, one performed right after a hardware master reset occurs) or a re-programming sequence (that is, one performed to change the protocol characteristics (Parity, rate, character length, etc.) after the device has been previously operating in the system). The programming sequence differs, in that, after a master reset, the chip is set to expect the first *control write* operation ($\overline{C/D}=1$) to contain a *mode instruction*. Any subsequent *control write* operations will be transferred to the *command instruction* register.

Now when it is desired to *change* the *mode instruction* register contents, the following re-programming sequence should be performed. A Command Control word of "40" Hex is written to the Chip. This turns off the Receiver and Transmitter and sets the IR (Internal Reset) bit. This bit causes the read/write control logic to expect the *next control write* operation to be a *new mode instruction*. After the new mode instruction is written to the chip, all subsequent control write operations will again be interpreted as *command instructions*. Therefore, after the *new mode instruction* is performed, the next command would turn the receiver and transmitter back on and resume normal Data operations.

AC ELECTRICAL CHARACTERISTICS

$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}; V_{CC} = 5.0\text{V} \pm 5\%; \text{GND} = 0\text{V}$

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
BUS PARAMETERS					
Read Cycle					
t_{AR}	Address Stable Before READ (CS,C/D)	50		ns	
t_{RA}	Address Hold Time for READ (CS,C/D)	5		ns	
t_{RE}	READ Pulse Width	350		ns	
t_{RD}	Data Delay from READ		200	ns	$C_L = 50 \text{ pF}$
t_{RDH}	READ to Data Floating		200	ns	$C_L = 50\text{pF}$
		25		ns	$C_L = 15 \text{ pF}$
Write Cycle					
t_{AW}	Address Stable Before WRITE	20		ns	
t_{WA}	Address Hold Time for WRITE	20		ns	
t_{WE}	WRITE Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for WRITE	100		ns	
t_{WDH}	Data Hold Time for WRITE	100		ns	
OTHER TIMINGS					
t_{TXC}	Transmit Clock Period	1.6		us	
t_{DTX}	TxD Delay from Falling Edge of TxC		200	ns	$C_L = 100 \text{ pF}$
t_{SRX}	Rx Data Set-Up Time to Sampling Pulse	200		ns	$C_L = 100 \text{ pF}$
t_{HRX}	Rx Data Hold Time to Sampling Pulse	100		ns	$C_L = 100 \text{ pF}$
f_{TX}	Transmitter Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	DC DC	500 600	kHz kHz	$C_L = 100 \text{ pF}$
t_{TPW}	Transmitter Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	1.0 800		us ns	
t_{TPD}	Transmitter Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	1.0 800		us ns	

Table 9 WD2123 A.C. PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
f_{RX}	Receiver Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	DC DC	500 600	kHz kHz	
t_{RPW}	Receiver Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	1.0 800		μs ns	
t_{RPD}	Receiver Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	1.0 800		μs ns	
t_{TX}	TxRDY Delay from Center of Stop Bit		8	t_{RXC}	$C_L = 50pF$ (16X)
t_{RX}	RxRDY Delay from Center of Stop Bit		$\frac{1}{2}$	t_{RXC}	
t_{IS}	Internal BRKDET Delay from Center of Data Bit		1	RXC	
t_{TRD}	TxRDY Delay from Falling Edge of WRITE		450	ns	
t_{TOD}	TXD Output from Falling Edge of WRITE		$1\frac{1}{2}$	t_{TXC}	
t_{WC}	Control Delay from Rising Edge of WRITE (RTS)		200	ns	
t_{CR}	Control to READ Set-Up Time (CTS)		1	t_{TXC}	

Table 9 WD2123 A.C. PARAMETERS

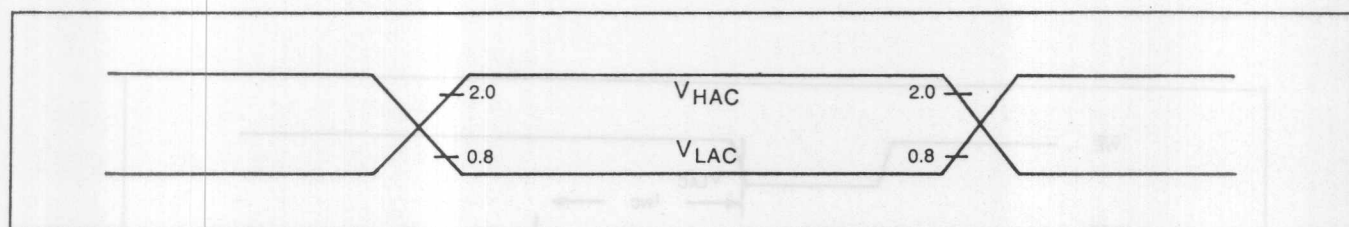


Figure 6 A.C. TEST POINTS

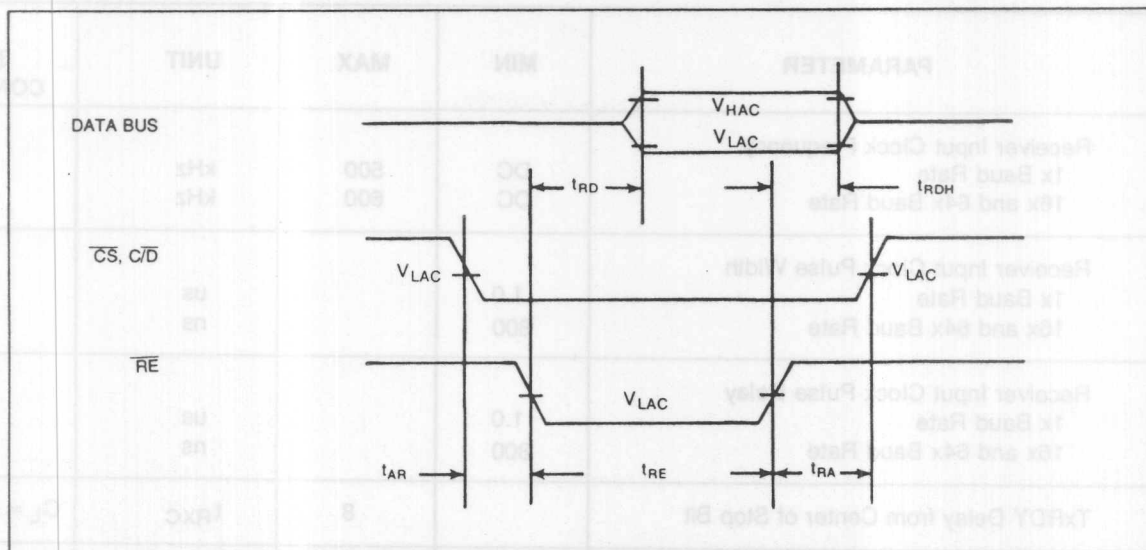


Figure 7 WD2123 READ TIMING

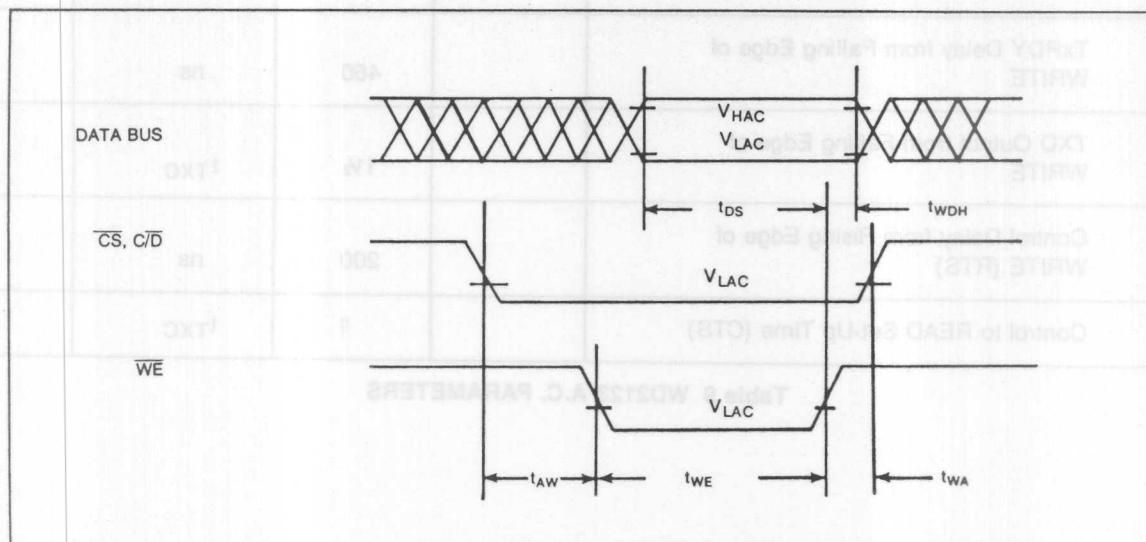


Figure 8 WD2123 WRITE TIMING

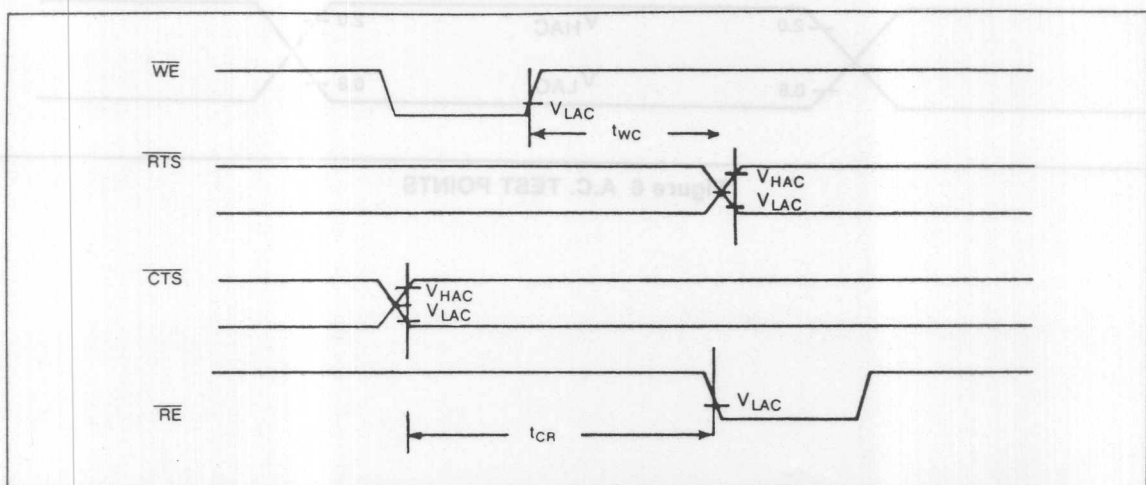


Figure 9 WD2123 INTERFACE CONTROL TIMING

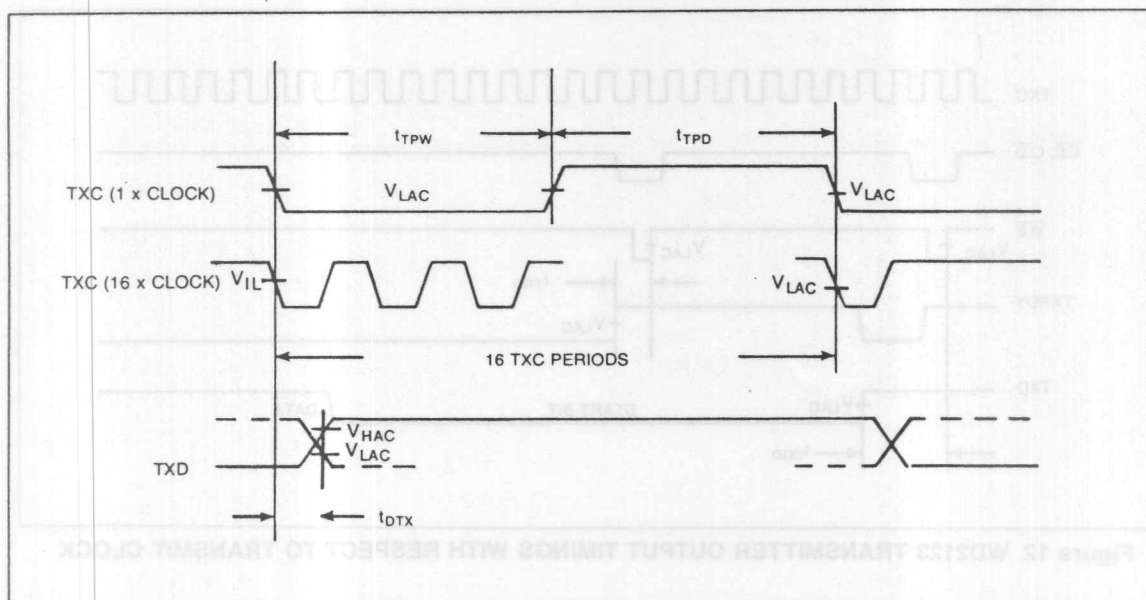


Figure 10 WD2123 TRANSMITTER CLOCK AND DATA TIMING

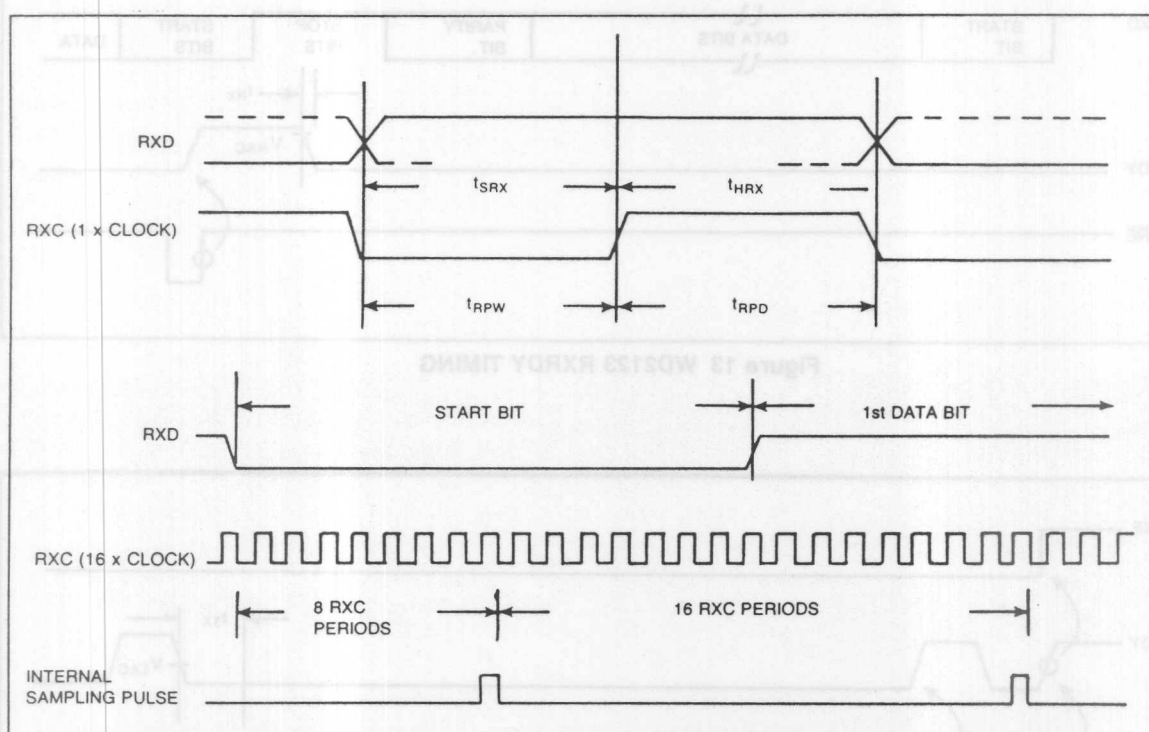


Figure 11 WD2123 RECEIVER CLOCK AND DATA TIMINGS

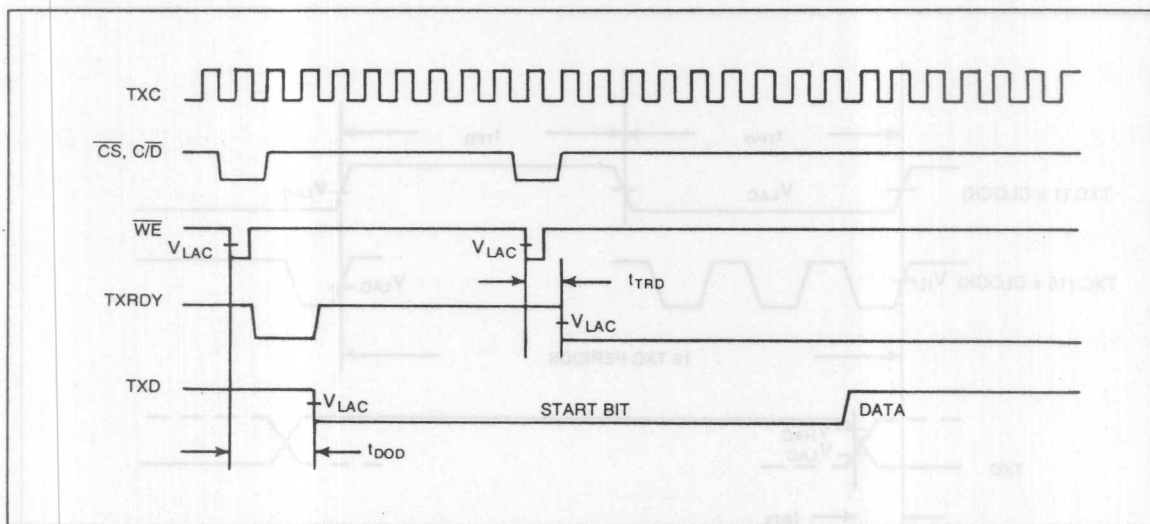


Figure 12 WD2123 TRANSMITTER OUTPUT TIMINGS WITH RESPECT TO TRANSMIT CLOCK

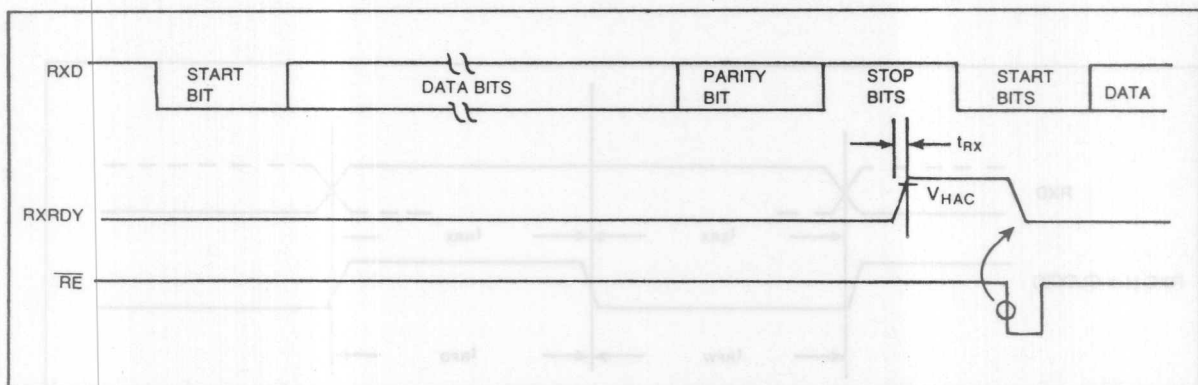


Figure 13 WD2123 RXRDY TIMING

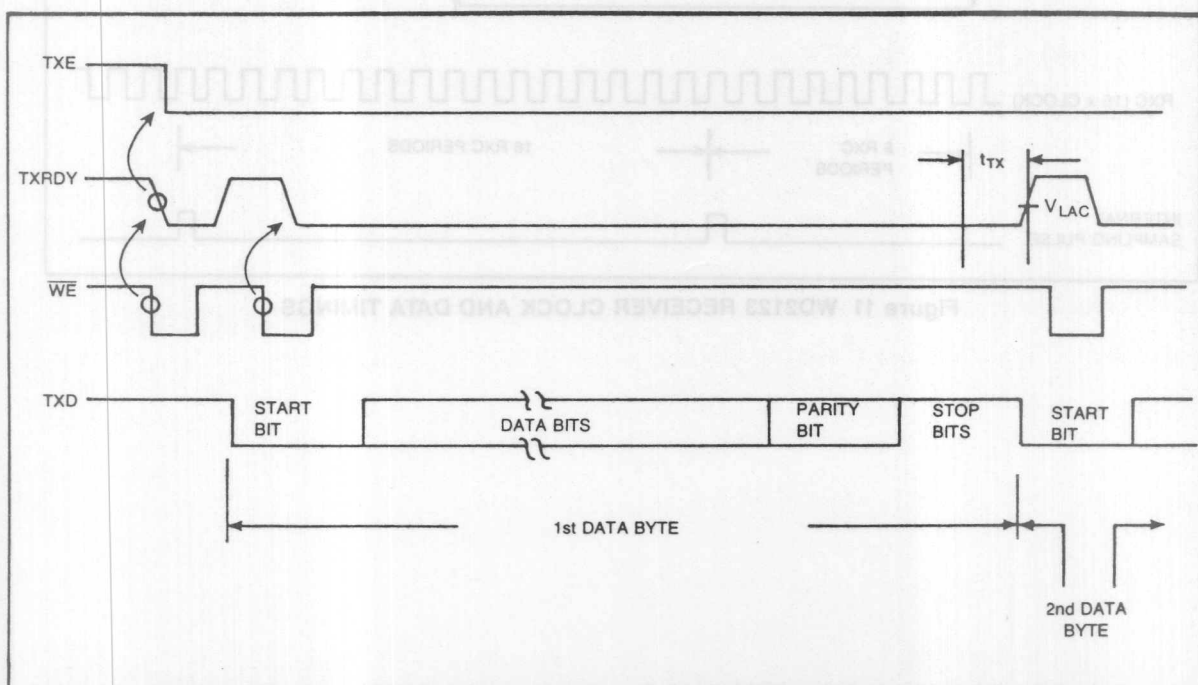


Figure 14 WD2123 TXRDY TIMING